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Density of states of short channel amorphous In–Ga–Zn–O thin-film transistor arrays fabricated using manufacturable processes

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The effect of temperature on the electrical characteristics of the short channel amorphous In–Ga–Zn–O (a-IGZO) thin-film transistor (TFT) arrays fabricated using manufacturable processes was investigated. This work shows that the fabricated TFT arrays are acceptable and stable enough for manufacturing of the ultra high definition (UHD) active matrix liquid crystal displays in size larger than 55 in. We observed that studied a-IGZO TFT arrays obeyed the Meyer–Neldel (MN) rule over a broad range of gate bias voltages. The MN rule and exponential subgap density of states (DOS) model were combined to extract the DOS distribution for the investigated a-IGZO TFT arrays. The results were consistent with the previous works on single a-IGZO TFTs. This study demonstrates that this method of DOS extraction can be applied to both single devices and arrays, and is reproducible from lab to lab. We believe that this approach of DOS extraction is useful for further development of UHD flat panel display technology. © 2015 The Japan Society of Applied Physics

1. Introduction

Since the successful demonstration of amorphous In–Ga–Zn–O (a-IGZO) thin-film transistor (TFT) on the flexible substrate at room temperature in 2004,[1] a large effort has been made to adopt a-IGZO as a TFT backplane for the next-generation flat panel display (FPD) including the active matrix liquid crystal displays (AM-LCDs) and light emitting diode displays (AM-OLEDs). Compared with the hydrogenated amorphous silicon (a-Si:H), which has confronted practical limitation in driving a large-size LCDs over 55 in. or 240 Hz ultra high definition (UHD, ~4000 × 2000) panels due to its low carrier mobility ($<1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$),[2] a-IGZO TFT with the practical field-effect mobility values exceeding $5\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ has emerged as a powerful active-matrix array alternative in industrial display production. Since 2013, the a-IGZO TFTs have been commercialized due to advantages such as a large area uniformity, a low temperature process, and compatibility with an existing a-Si:H TFT production line and equipment.[3–6] With the purpose of enhancing further the a-IGZO TFTs electrical characteristics and providing a better understanding about the device electrical stability, a number of studies have been conducted in past ten years. So far most of the studies including extraction of density of states (DOS) were done on a single insulated TFTs with a relatively large channel width (>100 μm) and length (>10 μm) to avoid a short channel effect. To our best knowledge, there is no published data on study of the short channel a-IGZO TFT arrays developed for the UHD panel to reflect realistic future display driving environment.

A-IGZO electrical performance such as a field-effect mobility, a threshold voltage, and a subthreshold swing is highly dependent on the localized subgap density of states.[7] Therefore, the determination of the DOS distribution can provide significant physical insight that will allow better device understanding leading to improved performance of the a-IGZO TFT manufactured panels. The extraction of DOS for a-IGZO TFT using the temperature-dependent characteristics has been established by Charlene et al.[8] and confirmed by Jeong et al.[9] This approach is based on the Meyer–Neldel (MN) rule and lately was successfully applied to different TFTs including a-IGZO,[10–12] ZTO/IZO,[13] and Cu_2O TFTs.[14] However, the efficacy of this approach has never been verified for fabricated a-IGZO TFT arrays using manufacturable processes. If successful, this approach can be used as a quality monitoring tool in the a-IGZO TFTs-based flat panel display mass-production.

In this work, through investigation of the temperature dependency of the TFT electrical characteristics, we extracted the subgap DOS based on the MN rule for the a-IGZO TFT arrays based on Cu gate and source/drain electrodes. This metallization will reduce the resistance–capacitance (RC) lines delay which is normally acceptable up to 20% of charging time. The TFT has back-channel etch (BCE) structure to reduce the number of photo-mask steps during fabrication and to enhance manufacturing yield. Also short channel dimension (channel width/length = 12/3 μm) was used to maintain a high pixel aperture ratio in ultra-high definition panels.

2. TFT arrays requirements for UHD AM-LCDs

Today there is increasing demand for UHD AM-LCDs with the panel size larger than 50 inches. Such panel performance cannot be achieved by hydrogenated amorphous silicon (a-Si:H) TFT without an advanced driving scheme because of a-Si:H TFT mobility limitations.[2] The poly-Si TFT active-matrix arrays could be used for UHD AM-LCDs but have a difficulty in obtaining uniform electrical properties over large areas caused by the grain structure and in achieving low manufacturing cost due to the expensive production cost and low manufacturing yield. Therefore, a-IGZO TFT active-matrix arrays appear to be very attractive solution for such application as long as their gate, source, and drain metallurgy has suitable characteristics such as low RC delays. For our specific case, we need to have a field-effect mobility and a RC delay: $>5\,\mathrm{cm^2\,V^{-1}\,s^{-2}}$,[15,16] and <0.8 μs (e.g., 20% of charging time of UHD, 120 Hz), respectively. Higher display resolution and frame rate require a shorter charging margin to be available for each pixel to complete charging, i.e., the RC delay must be minimized to allow the marginal signal charging. One possible solutions to decrease the RC delay is to adopt a low resistance metallurgy for the gate and source/drain electrodes. Today commonly used Al or Cr-based electrodes in display industry have confronted limitations to

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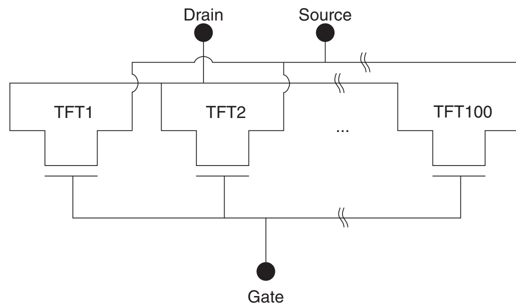

Fig. 1. Schematic diagram of the 100-TFT-array used to measure TFT electrical characteristics.

realize such a high resolution (large number of gate lines) and a large-sized panel.[17,18] Copper (Cu) based electrodes are considered as one attractive choice due to its low cost and a low resistivity (≈1.68 μΩ cm at 20 °C) [comparable to silver (Ag ≈ 1.59 μΩ cm at 20 °C)]. Devices discussed in this paper have Cu metallurgy. In addition, it has been experimentally shown by studying device dynamic response that a-IGZO TFTs are capable of supporting up to 8 K × 4 K resolution at 480 Hz.[19] Another requirement for UHD displays is to scale down the TFT channel dimension to acceptable level that will maintain or increase pixel aperture ratio to achieve a high transmittance rate and a low power consumption.[20] This channel dimension reduction should not have any impact on TFT array fabrication yield. The a-IGZO TFT arrays that satisfies above requirements were fabricated following the process described in Sect. 3 and were used for extraction of the distribution of DOS described below.

3. Experimental procedure

3.1 Fabrication

A-IGZO TFT arrays were fabricated in a well-controlled AM-LCD manufacturing line on the glass substrate as described in Refs. 2 and 4. The TFT has an inverted staggered bottom-gate back channel etched (BCE) structure. The Cu gate metal was deposited by DC sputtering and patterned by photolithography and subsequent wet-etching. Gate dielectric layer (SiN_x/SiO_x double layer) was deposited by plasma enhanced chemical vapor deposition (PECVD). The a-IGZO was deposited by conventional sputtering technique with optimized conditions so that it has In : Ga : Zn = 1 : 1 : 1 relative composition. The Cu-based source and drain electrodes were patterned by photolithography and subsequent wet-etching. Passivation layer (SiO_x/SiN_x double layer) was deposited by PECVD to prevent contamination from an ambient atmosphere. The studied array is composed of 100 same-structured TFTs which are connected in parallel as shown in Fig. 1. The channel width and length of individual TFT is about 12 and 3 μm, respectively. The measured total drain current (I_d) value was divided by 100 to obtain the average I_d value representing a single TFT. It should be noticed that the average TFT curves are similar to a single TFT, indicating very uniform and well defined TFT manufacturing process. We measured the transfer characteristics (I_d–V_{gs}) of the TFT array in the linear region ($V_{ds} = 0.1$ V) for temperatures ranging from 20 to 80 °C (10 °C interval). The device electrical performance was characterized by an Agilent B1500A semiconductor parameter analyzer in ambient air and dark conditions. The sample temperature was regulated by a heated chuck of the probe station. The measurements were repeated several times to acquire reproducible data.

3.2 Importance of evaluating TFT arrays

To assure the reliable display products to the customer and prevent the increase of the manufacturing cost, it is very important to have in place the quality control in the earlier stage of panel production and prevent the defective TFT devices from moving to next production step. As the pixel resolution increases, the importance of the uniformity of TFT arrays, instead of a single TFT, over the large area of mother glass becomes more and more critical. Therefore, during the manufacturing panel process, TFT arrays comprised of the large number of TFTs (50–100) connected in parallel are often patterned as a test element group (TEG) on the area outside of the display portion for testing the uniformity of TFT electrical characteristics. These TFT arrays can be used to check 1) the uniformity of TFT characteristics for a given fabrication process and 2) the quality of mass production by verifying the arrays reliability and production yield. The DOS extraction method described in this paper using the temperature dependent TFT arrays characteristics, which has been successfully applied to a single TFT in the laboratory unit,[8–14] can be used as a monitoring tool of the TFT arrays quality in the display manufacturable production line.

4. Results and discussion

4.1 Temperature dependence of TFT transfer characteristics

Figure 2 shows a representative transfer curves at different drain-to-source voltage (V_{ds}) and various temperatures at $V_{ds} = 0.1$ V. It can be observed that transfer characteristics shift to negative direction of gate voltages in the subthreshold region with the increasing temperature. The negative shift of threshold voltage was found to be reversible, i.e., when the temperature was decreased back to 20 °C, the transfer curve was able to recover to the initial state. The I_{off} change in the linear region ($V_{ds} = 0.1$ V) with the temperature cannot be observed in our experiment since I_{off} is below detection limit of used equipment. It should be noticed that a very low I_{off} will allow reduced power consumption of UHD AM-LCD.[6] The field-effect mobility (μ) and threshold voltage (V_{th}) were extracted using the standard MOSFET I_d–V_{gs} equation in the linear region ($V_{ds} = 0.1$ V):[21]

$$I_d = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{th})V_{ds}, \tag{1}$$

where C_{ox} is the gate insulator capacitance per unit area, W and L are TFT channel width and length, respectively. The fit range was chosen between 10 and 90% of the maximum drain current. Figure 3 shows a representative transfer curve and the 10–90% method used for extraction of the field-effect mobility and threshold voltage values. The subthreshold swing (SS) was taken as the average of three values nearest the maximum value in the subthreshold region using the following equation:

$$SS = \left(\frac{d \log I_d}{dV_{gs}}\right)^{-1}. \tag{2}$$

The TFT parameters as a function of temperature are shown in Fig. 4. It is clear from Fig. 4(a) that as the temperature

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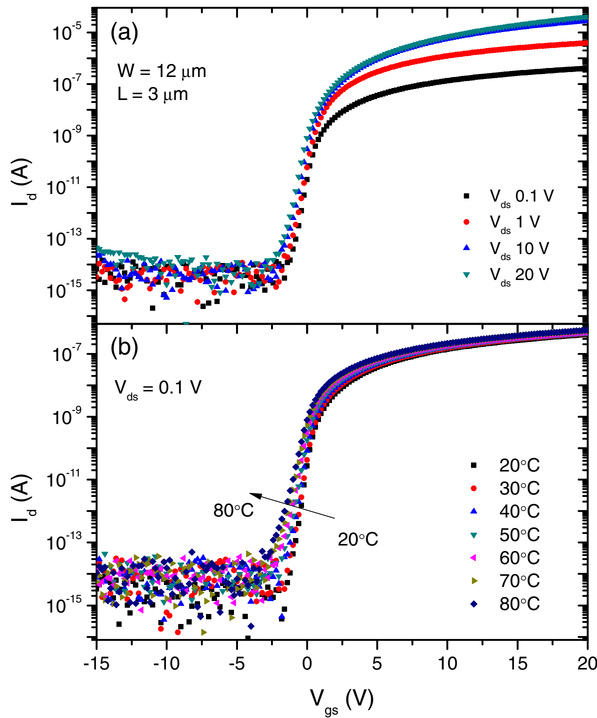

Fig. 2. (Color online) Average I_d–V_{gs} transfer characteristics in the log scale (a) measured at different V_{ds}, and (b) at various temperatures ranging from 20 to 80 °C.

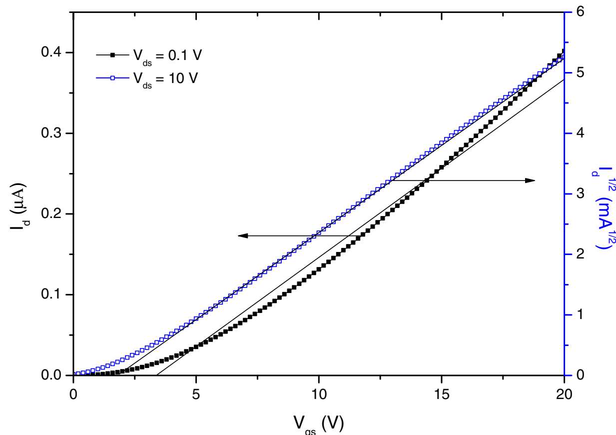

Fig. 3. (Color online) Representative average transfer curve of a-IGZO TFT array in linear scale. The linear fittings using 10–90% method to extract the field-effect mobility and threshold voltage are also shown.

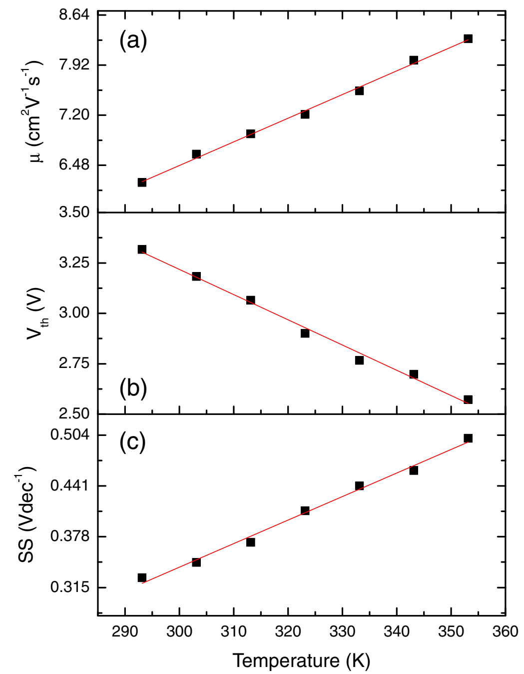

Fig. 4. (Color online) Temperature dependence of the (a) field-effect mobility, (b) threshold voltage, and (c) subthreshold swing.

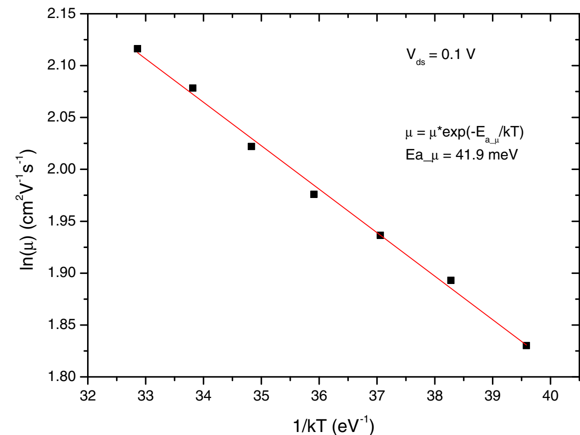

Fig. 5. (Color online) Temperature dependence of the field effect mobility extracted using 10–90% method.

increases from 20 to 80 °C, the field-effect mobility (μ) is thermally activated and increases from 6.2 to 8.3 $cm^2 V^{-1} s^{-1}$ with the temperature coefficient of 0.034 $cm^2 V^{-1} s^{-1} K^{-1}$. The obtained μ value is suitable for UHD AM-LCD. Figure 4(b) shows that the threshold voltage (V_{th}) decreases from 3.3 to 2.6 V with the temperature coefficient of −12.4 mV/K; this value is smaller than the one reported previously for a-IGZO TFT[8] or for a-Si:H TFT.[22] Figure 4(c) shows the subthreshold swing increases 0.17 V with the temperature with a temperature coefficient of 0.0029 $V dec^{-1} K^{-1}$. Observed steep subthreshold swing will allow fast transition between off and on state, which is important for UHD AM-LCD. It is noted that the field-effect mobility has a relatively low activation energy of 41.9 meV as compared to a-Si:H TFTs[22] as shown in Fig. 5. The activation energies of mobility (E_{a_μ}) were obtained using the following Arrhenius relationship:

$$\mu = \mu^* \exp\left(-\frac{E_{a_\mu}}{kT}\right), \tag{3}$$

where μ^* is the prefactor of this mobility, k is the Boltzmann constant, and T is temperature. The obtained μ^* value for our array is 32.8 $cm^2 V^{-1} s^{-1}$. This temperature dependency of μ and V_{th} can be explained by the multiple trapping transport mechanism[23] developed for a-Si:H TFTs. It is assumed that electrons that are thermally activated from the localized trap sites into the conduction band will contribute to a free carriers resulting in a higher mobility and smaller threshold voltage. At the same time, we expect an increase in density of gap states resulting in a larger subthreshold slope as experimentally observed. For oxide semiconductors, thermally excited electrons are mainly associated with the detrapping from the

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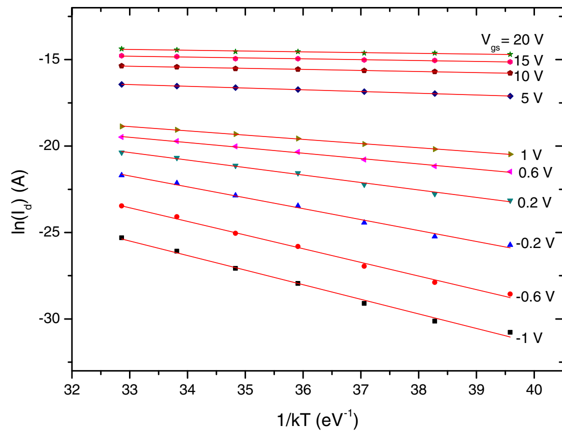

Fig. 6. (Color online) Temperature dependence of the drain current with different gate voltages.

sub-bandgap trap states and the generation of defects such as oxygen vacancies which can be increased by the thermal heating.[24–26]

4.2 MN rule

In this study, we found that a-IGZO TFT array also obeyed the MN rule. Figure 6 shows the linear relationship between $1/kT$ and $\ln I_d$ as a function of V_{gs}, which is described by

$$I_d = I_{d0} \exp\left(-\frac{E_a}{kT}\right), \quad (4)$$

where I_{d0} is the prefactor, and E_a is the activation energy. I_{d0} and E_a can be easily extracted by the least square fitting. It is well known that the MN rule is an intrinsic material property observed in number of disordered organic and inorganic semiconductors.[27] In the subthreshold region ($-1 < V_{gs} < 1.4$ V) the drain current I_d significantly changes with temperature, but in the above-threshold region ($V_{gs} > 1.4$ V) the variation of I_d is reduced. This means that two different TFT operating regimes can exhibit different MN relations, which is described by

$$I_{d0} = I_{d00} \exp(AE_a), \quad (5)$$

where I_{d00} is a constant, and A is the MN parameter. Figures 7(b) and 7(c) show that, as expected, E_a and I_{d0} exponentially decrease with V_{gs}. The activation energy E_a not only describes an average energy that the electrons need to gain to be released from the localized subgap states but also represents the energy difference between the Fermi level (E_F) and the conduction band edge (E_C) shown in Fig. 7(a). The E_a decreases with the increasing of the gate voltage since the V_{gs} increment makes the E_F move up to conduction band edge. Since the degree of E_F movement can be varied according to the distribution of DOS near the conduction band, the E_a can be correlated with the DOS in the sub-bandgap region. The minimum activation energy E_a(min) which represents density of conduction-band-tail states[21] is about 45 meV. This value will be compared with value obtained from the calculated DOS distribution. The prefactor I_{d0} exponentially increases with the increasing activation energy E_a as shown in Fig. 8. The I_{d0} has a linear relationship with the E_a over the broad range (0.1–0.8 eV). The derivative of I_{d0} with respect to E_a can show that MN parameter changes with E_a, e.g., V_{gs}, as shown in Fig. 9. We observe that A values have relatively well-defined two different regions, one ranging from 0.25 to 0.80 eV and another at ~0.25 eV corresponding to the deep-gap states and band-tail states, respectively. In general, the subgap DOS in the upper half above the E_F has been described by the combination of an exponential or Gaussian deep gap states and exponential band tail states.[28] As the V_{gs} increases, the E_F moves up through the deep-gap states first and then moves deeper into the band tail states. The E_a decrease accelerates within

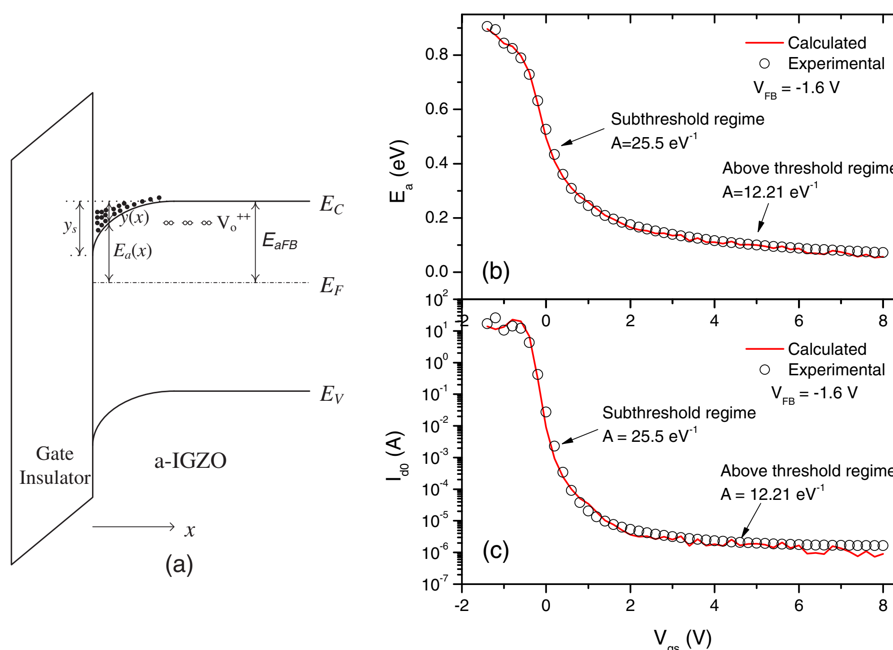

Fig. 7. (Color online) (a) Schematic energy band diagram of a-IGZO TFT near the gate insulator/a-IGZO interface and comparison of calculated and measured (b) activation energy E_a and (c) prefactor I_{d0}.

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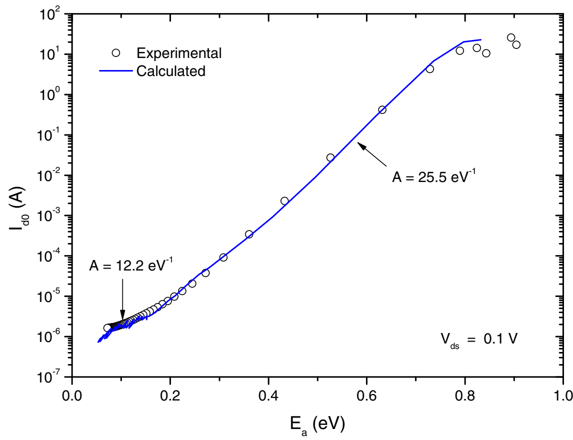

Fig. 8. (Color online) Experimental and calculated prefactor I_{d0} as a function of activation energy E_a.

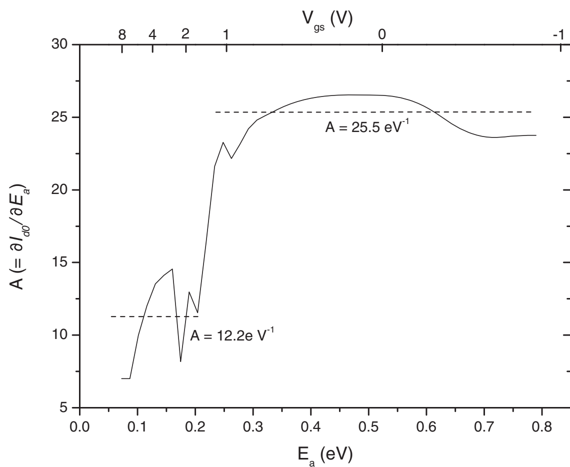

Fig. 9. Variation of MN parameter ($\partial I_{d0}/\partial E_a$) as a function of activation energy E_a.

relatively small V_{gs} range (−1.0 to 1.4 V) and the decreasing rate of E_a falls down rapidly afterwards as shown in Fig. 7(b), indicating that the E_F moves up faster in deep-gap states than band tail states. Even though the A values change with the V_{gs}, since A can be influenced by band-bending [$A = f(E_a) = f(f(V_{gs}))$], we selected two values of A corresponding to two different regions, e.g., deep-gap states and band tail states. This will allow simplify the DOS extraction using the least square fitting of I_{d0} and E_a. A of 25.5 eV^{-1} corresponding to the TFT subthreshold regime (deep gap states) was selected. For above threshold TFT regime (band tail states), A of 12.2 eV^{-1} was selected. Next the DOS was separately calculated in the subthreshold and above threshold TFT region.

4.3 DOS extraction

To obtain the DOS distribution for ultra-high resolution a-IGZO TFT arrays, the procedure described previously by Chen et al.[8] and Jeong et al.[9] for a single TFT was adopted and is briefly described. In this work, we also assumed that all electron charges are occupied in the localized states, and the probability of finding an electron at a certain energy level is determined by 0 K Fermi statistics. As shown in Fig. 7(a), the E_a is not only a function of V_{gs} but also a function of the distance x from the gate insulator/semiconductor interface. $E_a(x)$ is reduced by the band bending $y(x)$ induced by V_{gs} and can be expressed as $E_{aFB} - y(x)$, where E_{aFB} is the activation energy under flat band condition. The drain current $I_d(V_{gs})$ can be written as follows from Eqs. (4) and (5):

$$I_d(V_{gs}) = \frac{I_{FB}}{d_s}\int_0^{d_s} \exp\left[\left(\frac{1}{kT} - A\right)y(x)\right]dx, \qquad (6)$$

where d_s is the thickness of a-IGZO and $I_{FB} = I_{d00}\exp[(A - 1/kT)E_{aFB}]$ is the flat band current. First, to determine the amount of band bending $y(x)$ and the induced charge density n, Poisson equation should be solved for the electric field, i.e., applied gate voltage V_{gs}, given by

$$\frac{d^2y}{dx^2} = \frac{q \cdot n(y)}{k_s \cdot \varepsilon_0}, \qquad (7)$$

where q, k_s, and ε_0 are absolute value of the electronic charge, the dielectric constant of a-IGZO, and the permittivity of the free space, respectively. Then Eqs. (8) and (9) are derived using Grünewald et al.'s work.[29] The surface band bending $y_s(V_F)$ is first calculated from experimental drain current data $I_d(V_F)$ by the numerical iteration using the following equation:

$$\exp\left[\left(\frac{1}{kT} - A\right)y_s(V_F)\right] - \left(\frac{1}{kT} - A\right)y_s(V_F) - 1 = \frac{\frac{1}{kT} - A}{I_{FB}}\frac{d_s}{d_{ins}}\frac{k_{ins}}{k_s}\left[V_F I_d(V_F) - \int_0^{V_F} I_d(V_F')\,dV_F'\right], \qquad (8)$$

where d_{ins}, k_{ins}, and V_F are the thickness of the gate insulator, the dielectric constant of the gate insulator, and the difference between V_{gs} and the flat band voltage V_{FB} ($V_F = V_{gs} - V_{FB}$), respectively. Then, with the surface band bending calculated above, the induced surface charge density $n(y_s)$ is obtained by

$$n(y_s) = \frac{k_{ins}\varepsilon_0}{qd_{ins}d_s}\frac{I_{FB}\left\{\exp\left[\left(\frac{1}{kT} - A\right)y_s\right] - 1\right\}}{\frac{dI_d}{dV_F}}. \qquad (9)$$

Figure 10 shows the calculated band bending y_s at the semiconductor/insulator interface as a function of V_F and induced charge density n as a function of y_s with the flat band voltage $V_{FB} = -1.6$ V. The surface bend bending y_s increases with respect to V_F and therefore E_a decreases as shown in Fig. 7(b). This means that a smaller energy is required to detrap the electrons from the localized subgap states as V_{gs} increases. Charge density induced by the additional band bending from the flat band condition at the gate insulator/semiconductor interface increases exponentially according to Eq. (9). The appropriate V_{FB} is determined by comparing the experimentally extracted E_a as a function of V_{gs} with the theoretically calculated activation energy E_a given by

$$E_a(V_{gs}) = E_{aFB} - \frac{I_{FB}}{I_d(V_{gs})d_s}\sqrt{\frac{k_s\varepsilon_0}{q}}\int_0^{y_s}\frac{y\exp\left[\left(\frac{1}{kT} - A\right)y\right]}{\sqrt{2\int_0^{y} n(y')\,dy'}}dy, \qquad (10)$$

which is derived starting from Eq. (4) and its derivative with respect to $(1/kT)$, $E_a(V_{gs}) = -[1/I_d(V_{gs})] \cdot [dI_d(V_{gs})/$

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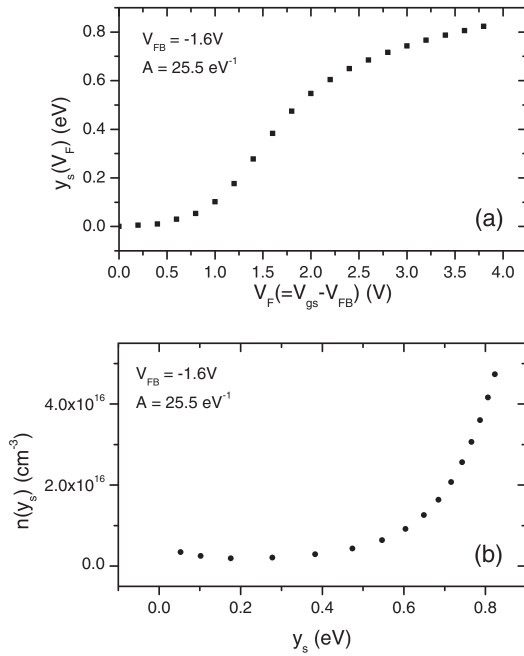

Fig. 10. (a) Calculated band bending y_s at the semiconductor–insulator interface as a function of V_F (= $V_{gs} - V_{FB}$) and (b) induced charge density n as a function of y_s in the subthreshold regime.

$d(1/kT)$]. The flat band activation energy E_{aFB} and the flat band current I_{FB} were simply found by interpolation at V_{FB} from experimental $E_a(V_{gs})$ data. The surface band bending y_s shape and the flat band voltage V_{FB} value can vary from sample to sample based on TFT fabrication processes and used materials.[8,9,11,14] Figures 7 and 8 show that the experimental data are well described by theoretical calculation when $V_{FB} = -1.6$ V, $E_{aFB} = 0.85$ V, and $A = 22.5$ and $12.2\,\text{eV}^{-1}$ in the subthreshold and above threshold regimes are used, respectively. We observe some negligible scattering of E_a and I_{d0} above threshold regimes in Figs. 7(b) and 7(c) which is caused by the term of derivative of I_d (dI_d/dV_F); this term may contain some noises associated with the measurement conditions that can affect derivation of the induced charge density in Eq. (9). From these results, we finally extracted the DOS distribution $N(E)$ from

$$N(E) = \left|\frac{dn(y_s)}{dy_s}\right|_{y_s=E}, \tag{11}$$

assuming 0 K Fermi statistics. Figure 11 shows the extracted DOS distribution as a function of the energy ($E - E_C$). Since the semi-log value of DOS has the linear relation with the energy ($E - E_C$) for both the subthreshold and above threshold regimes, the DOS distribution can be described by the exponential subgap-trap DOS model as

$$N(E) = N_C \exp\left(-\frac{E_C - E}{kT_t}\right), \tag{12}$$

where E_C is the energy level of the conduction band minimum, N_C is the trap density at E_C, and kT_t is the characteristic energy. The calculated DOS from the subthreshold regime (deep states) exhibits the value of $\sim 10^{18}\,\text{cm}^{-3}\,\text{eV}^{-1}$ with a characteristic energy of about 129 meV, which is consistent with the previous work[8] using temperature-dependent field-effect measurements. The DOS for above threshold regime

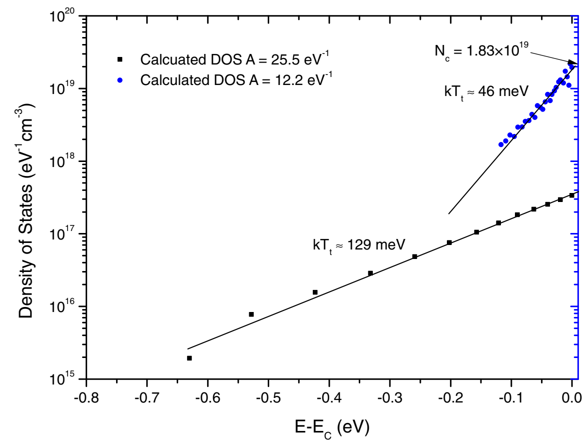

Fig. 11. (Color online) Calculated DOS distribution for both the subthreshold and above threshold regime as a function of ($E - E_C$).

(band tail states) is larger than that for subthreshold regime and has a steeper slope with a characteristic energy of about 46 meV. The trap density at the conduction band minimum N_C is $1.83 \times 10^{19}\,\text{cm}^{-3}\,\text{eV}^{-1}$. These results are also consistent with the previous experimental data obtained for a single a-IGZO TFT ($kT_t = 10$–150 meV, $N_C = 10^{17}$–10^{19} $\text{cm}^{-3}\,\text{eV}^{-1}$).[8–12,30–32] In general, it is expected that the DOS distribution can vary with the experimental and process conditions. The 0 K approximation for DOS extraction makes a small error only when the $N(E)$ is a slowly varying function with energy E. Since our results satisfy this condition, 0 K approximation in extracting the DOS is acceptable. It should be noted that the characteristic energy for above threshold regime ($kT_t = 46$ meV) has a similar value as the mobility activation energy ($E_{a_\mu} = 41.9$ meV) and the drain current minimum activation energy [$E_a(\min) \approx 45$ meV]. This demonstrates that the characteristic energy obtained from the DOS calculation using the temperature-dependent field effect measurements can be correlated with an average effective barrier height [Eqs. (3) and (4)] of the drain current conduction that is thermally activated. In addition, this result shows the validity of the DOS extraction using the two values of A representing the deep gap states and band tail states, respectively.

Since the DOS can affect the a-IGZO TFT electrical characteristics and stability, the determination of DOS is important for device and arrays control during process development. It was shown in this study that the DOS extraction method can be applied to UHD a-IGZO TFT arrays to be used for next generation of the flat panel displays. It is also clear that the DOS extraction method described in this paper can be used for both single TFTs and TFT arrays and can provide similar results but not identical from lab to lab. Therefore this approach can be used to explain the change of device/arrays electrical characteristics after an external bias-temperature stress. This DOS extraction method is simple and practical since it simply measures the temperature dependence of transfer curves. Another method to extract DOS is capacitance–voltage (C–V) methods,[31–33] but this approach cannot be used for our arrays since no reliable C–V curve can be measured for a short channel devices with a small overlap (<3 μm). Recent reliability studies[34–39] under external stress such as temperature, illumination, and electrical bias have

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suggested the variation of trap states near the conduction band edge associated with the oxygen vacancies or Zn interstitials could be responsible for threshold voltage shift. We think that the method described in this paper could be used to study DOS change induced by external stress.

5. Conclusions

This study investigated the effect of temperature on the ultra-high definition arrays of the a-IGZO TFTs. The mobility, threshold voltage, and subthreshold swing linearly changed with the temperature due to the thermally activated free carrier electrons. These device parameters appear to be acceptable and thermally stable for ultra-high resolution AM-LCDs. The DOS distribution in the bandgap was calculated using the temperature-dependent field effect data, based on the MN rule and 0 K Fermi statistics. The subthreshold and above threshold regimes were separately taken into account to calculate the deep and tail states. Combined with an exponential subgap trap model, the DOSs for the sub-threshold and above threshold regime are $\sim 10^{18}\,\mathrm{cm^{-3}\,eV^{-1}}$ and $1.83 \times 10^{19}\,\mathrm{cm^{-3}\,eV^{-1}}$ with characteristic energies of 129 and 46 meV, respectively. These values are much lower in comparison to those estimated for a-Si:H TFTs, and are consistent with those reported for single a-IGZO TFTs. This study confirms that the ultra-high resolution a-IGZO TFT arrays have a high performance and are appropriate for the application to UHD AM-LCDs.

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